Why the long-term charge offset drift in Si single-electron tunneling transistors is much smaller (better) than in metal-based ones: Two-level fluctuator stability

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A common observation in metal-based (specifically, those with AlO_x tunnel junctions) single-electron tunneling (SET) devices is a time-dependent instability known as the long-term charge offset drift. This drift is not seen in Si-based devices. Our aim is to understand the difference between these, and ultimately to overcome the drift in the metal-based devices. A comprehensive set of measurements shows that (1) brief measurements over short periods of time can mask the underlying drift, (2) we have not found any reproducible technique to eliminate the drift, and (3) two-level fluctuators (TLFs) in the metal-based devices are not stable. In contrast, in the Si-based devices the charge offset drifts by less than $0.01e$ over many days, and the TLFs are stable. We also show charge noise measurements in a SET device over four decades of temperature. We present a model for the charge offset drift based on the observation of nonequilibrium heat evolution in glassy materials, and obtain a numerical estimate in good agreement with our charge offset drift observations. We conclude that, while the Si devices are not perfect and defect-free, the defects are stable and noninteracting; in contrast, the interacting, unstable glasslike defects in the metal-based devices are what lead to the charge offset drift. We end by suggesting some particular directions for the improvement in fabrication, and in particular, fabrication with crystalline metal-oxide barriers, that may lead to charge offset drift-free behavior.
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I. MOTIVATION

There have been a variety of applications suggested for single-electron tunneling (SET) devices, based on the Coulomb blockade.[1] These applications include integrated circuit memory and logic,[2,3] based on the small size and low power potential of these devices. There are also applications in electrical metrology, including standards of capacitance, current, temperature, and others.[4–6]

For all of these potential applications, there is a practical difficulty with many implementations of SET devices: the long-term charge offset drift. This drift manifests itself as a time-dependent unpredictable instability in the device operation. As an example, let us consider a simple SET device: the SET transistor (SETT). In Fig. 1, we show the typical transistor control curve (drain current versus gate voltage) for both a standard field-effect transistor (FET) as well as for a SETT. The typical field-effect transistor has an "S-shaped" curve; the shape defines the basic digital nature of most electronics because, except for a narrow transition region, the current is either high or low (transistor is turned on or off). In contrast, the SETT has a periodic control curve, due to the nature of the Coulomb blockade: As schematically indicated in the figure, the period of the oscillation corresponds to putting one additional electron on average on the gate capacitor.

The periodic nature of the control curve in SET transistors, while providing the potential for the world's most sensitive charge electrometers, also presents a weakness in these devices: If there is a small change in the charge polarization induced on the gate capacitor by mobile charges in the nearby insulators, this can in an uncontrolled way turn the SET transistor from on to off or vice versa. It is commonly observed that there is indeed a random fixed offset to the control curve which is known as the "charge offset" Q_0; it is also commonly believed that charged defects are the source of Q_0.

Because the fixed charges in the nearby insulators are defects in the insulating matrix or lattice, there is usually an associated time-dependent fluctuation to the charge offset due to the motion of these defects. This observation is not

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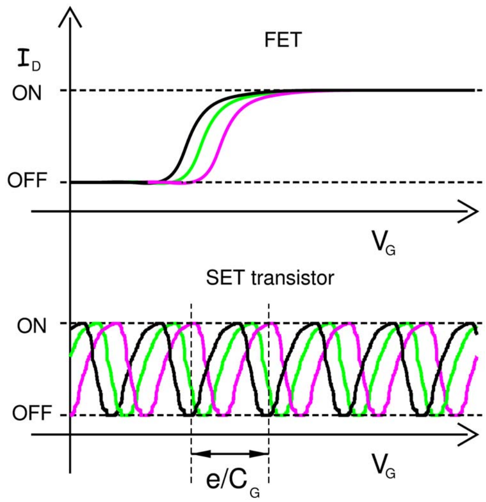

FIG. 1. (Color online) Illustration of difference between FET and SET transistors, in the context of charge offset drift. Upper panel: this shows the standard "S-shaped" control curve for a FET; note that a small change in the threshold voltage (different colors) does not affect the basic on/off behavior outside of the threshold region. Lower panel: in contrast, the basic control curve for a SET transistor is periodic, with a period corresponding to putting one more electron on the gate capacitor. Because of this periodicity, a small change in the charge offset can substantially alter the behavior of the transistor, turning an "off" state into an "on" state, and vice versa.

limited to the field of SET devices. Rather, there is a long history of both $1/f$ noise (due to the motion of a large number of mobile defects) and two-level fluctuators (TLFs) (due to the motion of a single dominant mobile defect) in a wide variety of metallic[7] and semiconducting[8] devices.

Considering specifically SET devices, we have previously shown that there are two general classes of time-dependent random fluctuations in $Q_0(t)$.[9,10] The first class corresponds to small, stationary $1/f$ noise; the typical total size of fluctuation over the experimental bandwidth is about $10^{-3}e$ (e is the fundamental electron charge). The second class is the long-term drift, which typically occurs over periods of hours or longer. The drift is typically nonstationary, with a size of a substantial fraction of $1e$, and can be much greater than $1e$ in some cases.

What is the effect of these two classes of noise? The $1/f$ noise, as is common in active devices, limits the resolution of the SET transistor as a very sensitive charge electrometer. In contrast, the long-term drift has a more deleterious effect: Because it can shift the control curve of the transistor by a large fraction of $1e$, as schematically indicated in Fig. 1, the drift can unpredictably change the transistor from on to off. Thus, the long-term drift can preclude integration of SET devices. Another example of the deleterious effect of the long-term drift is in the metrology application: Here, the drift prevents a charge pump from being used for more than a few hours continuously; after this time, the pump must be retuned to suppress the effect of the drift.

As a general observation, the long-term drift is prevalent in SET devices based on the Al/AlO_x/Al tunnel junctions (in general, the measurements reported herein for "metal-based devices" are specifically for Al/AlO_x/Al tunnel junctions; we will use the two terms interchangeably, to contrast with the Si-based devices). There have been two anecdotal reports of such devices which appeared to have no long-term drift.[11,12] For the second report,[12] we will show data for $Q_0(t)$ from a device fabricated by the same group at the same time; unfortunately, this device also showed long-term drift. This subsequent remeasurement demonstrates one of the important points of this paper: In order to demonstrate a lack of long-term charge offset drift in a particular class of devices, it is necessary to do a comprehensive set of measurements over multiple devices in different experimental conditions. This is because the nonstationary, hysteretic nature of the drift means that sometimes a particular device can exhibit no apparent drift for a limited amount of time; this fact can mask the overall existence of the long-term drift in a class of devices if one does not perform comprehensive measurements.

In contrast, as we have previously shown,[10,13,14] in at least one class of Si-based SET transistors, there is no apparent charge offset drift $[\Delta Q_0(t) \leqslant 0.01e]$. This fact forms one of the advantages of Si-based SET devices, and one of our aims is to determine how to attain such a lack of long-term drift in the metal-based SET devices. This fact is also puzzling for the following reason: It has been known for two decades that large TLFs are present in most Si nanodevices (of which SET devices are only a small fraction).[8] Since SET transistors are more sensitive to charge motion than other Si nanodevices, it is natural to wonder why the charge offset drift does not reflect the deleterious effect of the TLFs.

Thus, this paper aims to develop answers to the following questions:

(1) What is the basic mechanism that leads to long-term charge offset drift in most or all metal-based devices?
(2) What is the crucial difference between Si-based and metal-based devices that leads to the difference in $Q_0(t)$?
(3) Are there TLFs in the Si-based transistors? If so, why do they not cause charge offset drift?
(4) Can we, and if so how, attain a lack of charge offset drift in metal-based devices?

We will formulate answers to these questions as follows: In the next section of this paper, we will present a comprehensive set of measurements of $Q_0(t)$ in metal-based devices. Since the drift is device-specific, we have measured devices from several groups in order to sample as wide a range of behavior as possible. This set includes a compendium of a large number of measurements of devices made by one of the groups, as compiled over several years. This compendium will illustrate some of the typical features of the long-term drift, including the possibility that in some devices the drift may appear to be absent for specific realizations. We also include data from devices made by two other groups, one of which corresponds to a device from the same batch that previously did not exhibit any drift.[12]

Unfortunately, we have not identified as yet a way to make metal-based devices that have no charge offset drift. Thus, our conclusion at present is that there is a fundamental difference between the two classes of devices.

In the following section, we will present data and a compendium demonstrating the lack of charge offset drift in our Si devices, as fabricated at two different locations. We will also show the temperature dependence of noise between 0.02 and 300 K, in one device. One of the striking results from this measurement is that, although there are TLFs present in our device, those TLFs are completely stable. By this, we specifically mean that if we make wide temperature excursions and then return to the original temperature the same TLF is present with the same frequency dependence. This is in marked contrast to most metal-based devices, and we believe is the crucial difference that leads to a lack of charge offset drift in the Si-based devices.

Finally, in the last major section of this paper, we consider a model for the physical basis of the charge offset drift in the metal-based devices. This model is based on the results from the two-level systems (TLS) field as studied over several decades in glassy and amorphous materials.[15] Using the results of these studies, we can predict an amplitude and time dependence of the charge offset drift $Q_0(t)$ that seems to be in good quantitative agreement with the typical observation.

II. MEASUREMENT OF $Q_0(t)$ IN METAL-BASED TRANSISTORS

A. Experimental details and examples

As is standard in this field, we measure the charge offset drift as follows: We can repeatedly measure the control curve as schematically indicated in the lower panel of Fig. 1. By assigning a phase to each control curve measured in time, we can then compile the time dependence $Q_0(t)$. In the data discussed in this paper, some of the $Q_0(t)$ curves were obtained by repeatedly measuring the SET transistor control curve, and then subsequently fitting a sinusoidal shape to the curve to extract the phase (measurement method I, with a typical statistical uncertainty of $\pm 0.01e$). In other cases, we held the gate voltage constant and used a feedback circuit to apply an offset to the gate voltage V_G in order to keep the current I_D constant (measurement method II, with a typical statistical uncertainty of $\pm 0.001e$). In those cases, by normalizing the feedback voltage by the period of the oscillation, we were then able to obtain $Q_0(t)$.

In all cases discussed here for metal-based transistors, the measurements were performed near the base temperature of our dilution refrigerator, with an indicated temperature of about 0.02 K. By fitting the standard theory[16] to the data, we can extract the effective temperature of the electrons; we note that, at the typical current level $I_D \approx 1$ nA, this temperature is typically between 0.25 and 0.3 K. Generally, the large temperature rise of the electrons is due to the large electron-phonon thermal resistance present at low temperatures.

Figure 2 shows an example of a measurement of $Q_0(t)$ over a few days. We note that there is a TLF present with a small amplitude, and that near 19.1 there was an excursion for a short period of time. Other than that, this is an example of apparently small charge offset drift: Q_0 varies by only about $0.1e$ over several days. In the absence of other data, we would conclude that this device has quite a good charge offset drift behavior. In particular, we note that if we had only

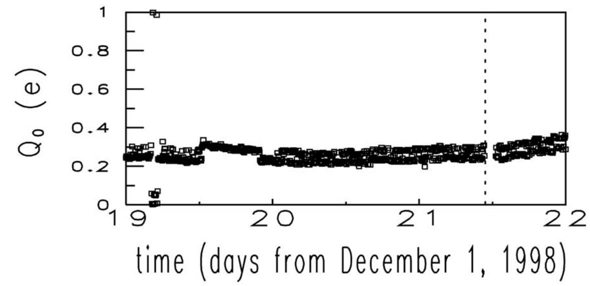

FIG. 2. Example of time dependence of Q_0 for a limited segment of run 2.10 ($Al/AlO_x/Al$), using method I. We note that there is a TLF present, with an amplitude of about $0.1e$. Over the course of this three-day measurement, except for one very short time near 19.1, the charge offset appears to be stable — neither drifting nor jumping. These data correspond to 2.10F in Table II. We note that, in this and all other data plots, the statistical uncertainty error bar is too small to be seen.

done a few measurements of the control curve over this time, we would have concluded that there was very little drift in this device.

Figure 3 shows the entire set of time-dependent charge offset measurements for the same device shown in Fig. 2; the

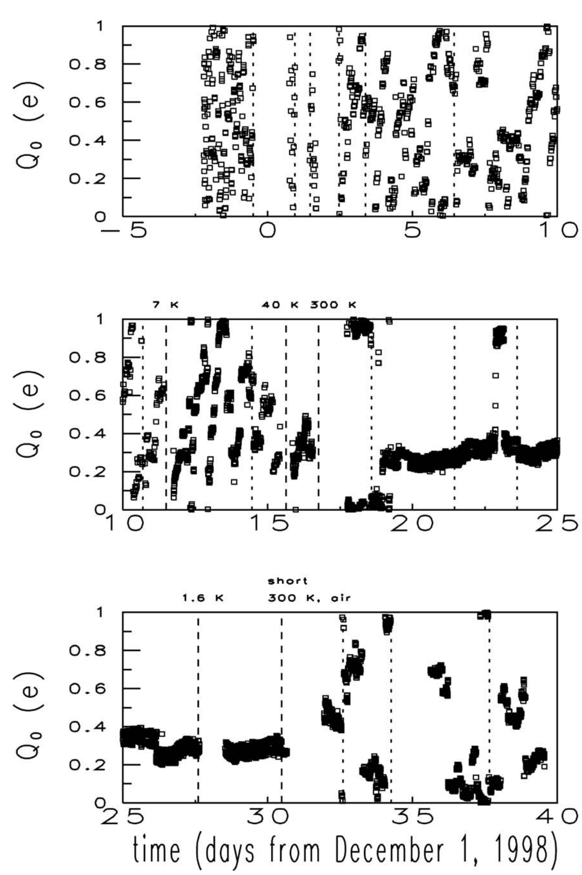

FIG. 3. Time dependence $Q_0(t)$ for all of run 2.10, using method I ($Al/AlO_x/Al$). The data in Fig. 2 are encompassed here between days 19 and 22 in the middle panel. The vertical dashed lines refer to deliberate temperature excursions or other events, as noted in the text above each panel. The vertical dotted lines mostly refer to mechanical events in the dilution refrigerator (specifically, transfer of liquid helium); in the upper panel, the first three dotted lines refer to accidental losses of data. Since the control curve for a SETT, as illustrated in Fig. 1, is periodic, we can only measure Q_0 modulo $1e$; for the particular set of data shown here, the monotonic drift in the first 15 days suggests that Q_0 in fact changes by many e.

data in Fig. 2 corresponds to the region between days 19 and 22 on the horizontal axis. This figure shows measurements on the same device over the course of about 1 1/2 months, during which there were several deliberate excursions of temperature, as shown above the top of each panel. In most cases, the sample was kept in vacuum with unchanging electrical conditions during these excursions. In the period between days 30.5 and 32, the device was not only warmed to room temperature, but the electrical leads were also shorted and the device was exposed to air.

Figure 3 illustrates several themes that we have observed multiple times:

(1) It is obvious that for the first 15 days or so there is an evolution from very rapid, sometimes monotonic, drift in $Q_0(t)$ to a much slower, sometimes stable behavior. We call this type of one-time evolution the "transient relaxation;" this is a fairly typical (but not always seen) behavior in the metal-based devices, and we will discuss it in greater detail in the section where we consider a model for the charge offset drift.

(2) After the transient relaxation, there was a period of about 10 days (from 19 to 30) where, except for one brief period at about day 23, the charge offset Q_0 was constant within about $0.1e$. This specific set of data is one of the best that we have ever observed for a metal-based device (see Fig. 4 for another).

(3) After a further temperature excursion, $Q_0(t)$ returned to a more typical behavior, stable and often constant over the course of about a day or less, with hysteretic jumps (discrete, nonsmooth jumps which do not repeat) or drifts at other times.

This last observation and the consideration of Fig. 2 in the context of Fig. 3 are both examples of the same theme: *In order to demonstrate convincingly that a particular device or class of devices has no charge offset drift, it is necessary to do a comprehensive set of measurements over an extended period of time.*

B. Measurements of $Q_0(t)$ in devices fabricated by other laboratories

All of the measurements reported herein were performed in the same cryostat located in NIST, Gaithersburg, MD, USA. It is quite evident from different anecdotal reports that the behavior of the charge offset drift $Q_0(t)$ depends markedly on the specific device. Because of this, we desired to measure devices fabricated by as wide a range of laboratories as could be achieved.

Figure 4 presents data from a device fabricated at the Physikalisch-Technischen Bundesanstalt (PTB) located in Germany. We note that, interestingly, this device was fabricated eight years before our measurements were performed; this may be the oldest SET device for which a measurement has been reported. There has been a previous report,[12] for a device from the same batch measured about two years after fabrication, that no charge offset drift appeared over a short measurement time of a few days. One difference between these devices was that the previously reported device had an

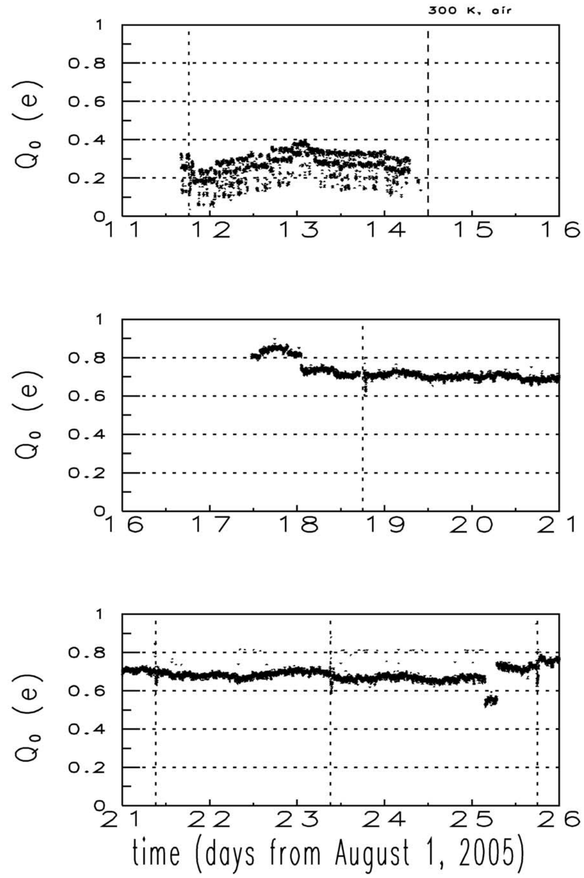

FIG. 4. Measurement of $Q_0(t)$ for a device fabricated at PTB in Germany, using method I ($Al/AlO_x/Al$). This data are denoted in the tables as 2.42B, C. Between 14.5 and 17.5 days, the device was warmed to room temperature and opened to the air. The measurement temperature was between 0.03 and 0.08 K. The vertical dotted lines refer to transfer of liquid helium.

Al film thickness of 60 nm, and the one reported in this paper was thicker, at 150 nm; if relaxation of film stress (see Sec. V) is a cause of the drift, this could be an important difference, with the thicker film having more drift. The behavior of $Q_0(t)$ in this figure is similar to those in the previous section, which were measured on devices fabricated at NIST, Gaithersburg, MD, USA. In particular, there is one fairly stable TLF which appeared and then disappeared (between 11.7 and 14.2 days), as well as several hysteretic jumps. There is also an overall slow drift in what would otherwise appear to be a stable value (for instance between about 20 and about 25 days).

Similarly, Fig. 5 shows the results of measurements on a device fabricated at NIST in Boulder, CO, USA. This figure shows features similar to the previous figures for devices fabricated both at PTB and at NIST, Gaithersburg, MD, USA.

C. Comparison of all measurements of $Q_0(t)$ in metal devices

Table I shows a compendium of results for a variety of devices measured over a range of times, as sorted by grade [i.e., from top to bottom by increasing amounts of charge offset drift $Q_0(t)$]; most devices were fabricated at NIST, Gaithersburg, MD, USA. The two devices fabricated at other

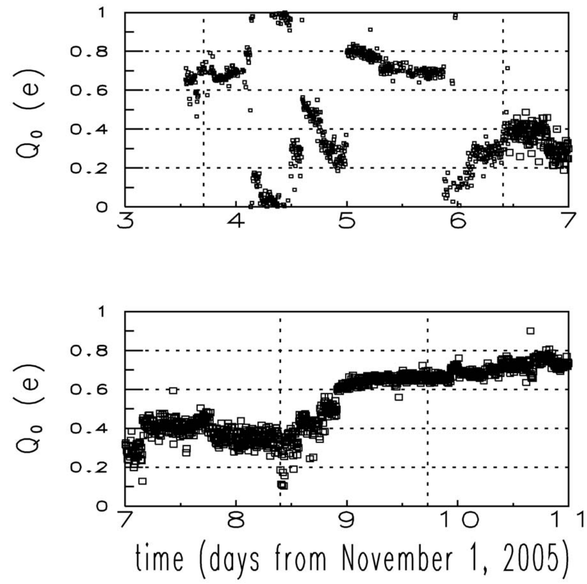

FIG. 5. Measurement of $Q_0(t)$ for a device fabricated at NIST in Boulder, CO, USA, using method I ($Al/AlO_x/Al$). This data are denoted in the tables as 2.45. The measurement temperature was between 0.15 and 0.30 K. The vertical dotted lines refer to transfer of liquid helium.

laboratories are listed at the beginning. We have included a large number of details in these tables, some of which are not discussed further in this paper. We note that our motivation for listing this large number of details is that it may be helpful to some researchers in the field, either because it may give them information as to what avenues are or are not promising, and also because other researchers may perceive useful correlations in the data.

Over the course of about 2 1/2 years, we attempted a variety of geometry and materials preparation techniques[9] in order to suppress or eliminate the charge offset drift. We were unsuccessful in finding a technique that would comprehensively reduce the amplitude of $Q_0(t)$.

In particular, we consider the column entitled "Q_0 behavior." A comprehensive set of measurements such as we have done show that, although in a particular device it may be possible to see stable or constant Q_0 for a few days, unfortunately, the general trend is that the charge offset Q_0 is not reliably constant for any device or any batch of devices.

Consideration of this compendium reveals the following trends:

(1) Parameters which affect the amount of charge offset drift:

Extra insulator deposition. "caged" devices and devices with "blankets" which typically have worse charge offset behavior than those without.

Transient relaxation devices which exhibit a relaxation not surprisingly having more drift.

(2) Parameters which do not appear to affect the charge offset drift:

Speed and electrical conditions upon cooldown. There have been anecdotal (unpublished) results reported that, if one cools the device more slowly or has a particular electrical condition applied to the device, the noise in a SET transistor may be greater or smaller. We see no evidence for dependence of $Q_0(t)$ on these parameters.

Normal/superconducting Al. We do not see a strong dependence on this parameter. It is arguable that perhaps devices in the superconducting state have better performance, but this is at present unclear.

Year of fabrication. We do not see any systematic trends with year, suggesting that a drift in parameter such as deposition system base pressure, quality of oxide, etc., is not affecting the overall lack of improvement in $Q_0(t)$.

Table II shows the same set of information sorted by date. In this context, we can consider the transient relaxation: measurements which exhibited such a relaxation have a gray background in the table. Examination of the table reveals the following trends.

Date of fabrication. In general, the transient relaxation only occurs when the fabrication (more specifically, the deposition) occurred no more than about two days before cooldown. We note that this general trend was violated in one case: run 2.10C.

Recurrence of transient relaxation. In no case did a thermal cycle up to 300 K or even to 350 °C cause a recurrence of the transient relaxation.

Materials preparation. Examination of runs 2.19A, 2.20A, 2.23A, 2.24A, and 2.25A all reveal that the transient relaxation is much more likely when the device had a deliberate deposition of extra insulating material on the island (caged devices or devices with blankets).

We will have more to say about these observations in Sec. IV, in which we describe the model for the charge offset drift in the metal-based devices.

D. Summary

A brief summary of the results is given in this section.

(1) In order to convincingly demonstrate a lack of long-term charge offset drift, comprehensive measurements over a long period of time are necessary.
(2) We have not found a reproducible way to eliminate the charge offset drift in metal-based devices; the typical behavior involves slow drift or hysteretic jumps.
(3) Extra insulating material degrades the behavior of $Q_0(t)$, while speed of cooling, electrical conditions, and normal/superconducting state do not.
(4) The transient relaxation often occurs; it appears to be associated with time since fabrication, and with the presence of extra insulating material.

III. MEASUREMENT OF $Q_0(t)$ AND TLF STABILITY IN SI-BASED TRANSISTORS

A. $Q_0(t)$

In contrast to the results in metal-based transistors, we have found that in the Si-based devices the charge offset is

TABLE I. Compendium of a large number of measurements of $Q_0(t)$, mostly on devices fabricated at NIST, Gaithersburg, MD, USA, sorted by grade [amount of $Q_0(t)$ drift]. Rows with gray background correspond to measurements where a transient relaxation was observed. Columns: "Q_0 grade" represents a rough ranking of the amount of $Q_0(t)$; "A" corresponds to very little drift. "Notes:" "Inline" and "angled" correspond to source and drain leads parallel to or perpendicular to island; "caged" refers to a device in an electrostatic cage (Ref. 9). "Fabrication details:" Dates refer to dates of fabrication; specific times refer to time of deposition of Al/AlO$_x$/Al; for device WH72-2 in run 2.20A, the tunnel junctions were fabricated by oxidation in ozone; "blanket" devices refer to transistors with a layer of deposited AlO$_x$ on top of either the tunnel junction or the center of the island. "Precondition:" Amongst other treatments were annealing at 350 °C in either N_2 or forming gas (mixture of N_2 and H_2). "Cooldown details:" Mostly these give the date and time when we reached a particular temperature; "illuminated" refers to an experiment where we exposed the device to light from a light emitting diode (LED) at base temperature. "Norm/sc" refers to normal or superconducting state. "$\sqrt{S_Q}(10\ \mathrm{Hz})(e/\sqrt{\mathrm{Hz}})$" refers to a measurement of the power spectral density of the short-term (typically $1/f$) noise at 10 Hz.

Fab location	Run	Q0 grade	device	meas't dates	notes	fabrication details	pre-condition	pre-cooldown electrical	cooldown details	norm/sc	I_{SD} (nA)	transient?	Q_0 behavior	$\sqrt{S_Q}$ (10 Hz) ($e/\sqrt{\mathrm{Hz}}$)
PTB	2.42B, C	A-	SL-66 44	8/11 - 8/27/05	inline	Al 150 nm, 1997		unshort 4 K	4 K, 300 K air, 4 K	norm	0.14	no	0.15 e 9 days	
NIST, Boulder	2.45	B	6-3-05 1	11/4 - 11/12/05		6/2/2001		unshort 4 K	none	norm	5.1	no	linear drift 0.1 e over 2 days	
NIST, G'burg	2.10F	A-	SM 1-1 19-21	12/17 - 12/30/98			300 K (vac) 8 hrs	left running		sc		no	3 TLFs in 14 days (1 in 12 days)	
	2.13E	A-	SM 3-13 19-21	4/30 - 5/6/99			350 C N_2 4/28 1400	unshort 4 K?	two days 100 K	sc	0.4	no	0.1 e 2 days, mostly flat	<~ 4 X 10^{-4} (not 1/f)
	2.14A	A-	SM 3-3 13-15	6/15 - 7/14/99		3/7/98; chip broke once	77 K 3/8/99, dry box 2 1/2 mth, 77 K 5/28 - 6/13	unshorted room temp	77 K 1 day, 4 K, 300 K, base **illuminated**	norm	0.5	no	flat 6 final days	
	2.18	A-	WH67-17 17-20	12/22/99 - 1/5/00	uncaged	12/14/99 1400	77 K 1/2 hr 12/15	unshort base	2 K, 300 K, 4 K,	sc	0.13	**NO**	0.1 e 5 days	
	2.18C	A-	WH67-17 17-20	2/4 - 2/14/00	uncaged	12/14/99 1400	77 K 1/2 hr 12/15	unshort base	immediately foll-	norm	0.13	no	0.1 e 4 days	1.0 X 10^{-3}
	2.20A	A-	WH 72-2 17-20	3/15 - 4/5/00	uncaged	3/13/00 1100	cold 3/14 1800	unshort base		norm	0.14	no	0.1 e 5 days	0.5 X 10^{-3}
	2.10G	B+	SM 1-1 19-21	12/31/98 - 1/8/99			300 K (vac) 10? hrs in air 1 hour	short, warm, cool, unshort		sc	0.7	no	0.1 e 1 day typical	
	2.13B	B+	SM 3-13 19-21	4/2 - 4/9/99			300 K (in vac?)	unshort 4 K?		sc	0.4	no	0.1 e 1 1/2 days	
	2.13D	B+	SM 3-13 19-21	4/14 - 4/16/99			300 K (twice)			sc	0.4	no	0.05 e 1 1/2 days	
	2.18	B+	WH67-17 13-16		caged	12/14/99 1400	77 K 1/2 hr 12/15	unshort base	50 K, base 3 days	sc	0.7		drifting, 0.1 e 1 day best	
	2.19A	B+	WH 72-10 17-20	2/23 - 3/13/00	uncaged	2/21/00 1800	cold 2/24 1900	unshort 1.6 K		norm	0.2	no	0.1 e 2 days	1.0 X 10^{-3}
	2.10H	B	SM 1-1 19-21	1/13 - 1/14/99			anneal 350 C N_2	short, warm, cool,		sc	0.8	no	0.2 e 1 day	
	2.13A	B	SM 3-13 19-21	3/8 - 4/1/99	(angled)	100 nm/65 mT/90 nm hanging by wires; base 9 X 10^{-6} depo 2 X 10^{-5}; 3/7/99		unshort 4 K	3/8 1200 77 K 3/9 1100 4 K 4 and 35 K later	sc	0.4	yes	0.1 e 1 day best	
	2.17	B	WH66-18 5-8	11/12 - 11/19/99	uncaged	10/28/99; base 1.7 X 10^{-7},	7 days room temp	unshort 4 K.	4 K 3 days?	norm	0.7	no	0.1e 2 days best, lots of drifting	1.0 X 10^{-3}
	2.22A	B	WH 79-16 13-15	7/12 - 7/18/00	inline	7/11/00; base 6 X 10^{-6}	cold 7/22 2200	unshort base		norm	0.03	no	0.1 e 1 day	
	2.23A	B	WH 72-8 16-18			7/22/00; no blanket	cold 7/23 1800	unshort base		norm	0.18	no	0.1 e 3 days	0.7 X 10^{-3}
	2.10C	B-	SM 1-1 19-21	11/27 - 12/9/98			300 K in vac 2 days?	unshort 0.29 K	4 K 11/27 1700	sc	0.8	yes (3 days)	best 0.2 e 1/2 day	
	2.10D	B-	SM 1-1 19-21	12/11 - 12/15/98			7 K less than 6 hours	?		sc	0.8	no	0.1 e 1/4 day	
	2.10E	B-	SM 1-1 19-21	12/15 - 12/16/98			40 K less than 8 hrs	?		sc	0.8	no	< 0.1 e 0.2 day	
	2.13F	B-	SM 3-13 19-21	5/7 - 5/13/99		rewire 5/7 1100	350 C H_2 5/7 1000	unshort 4 K?	4 K 5/7 1730	sc	0.4	no	0.2 e 2 days, drifting	
	2.17	B-	WH66-18 9-12	11/17 - 11/18/99	caged	depo 2.6 X 10^{-7}	7 days room temp	unshort 4 K.	4 K 3 days?	norm	0.7		0.2e 1/4 day	
	2.22A	B-	WH 79-16 16-18			7/11/00; base 6 X 10^{-6}	cold 7/22 2200	unshort base		norm	0.03	no	0.1 e 0.5 day	
	2.25A	B-	WH 72-21 7-9		"	blanket center, island on top	cold 9/29 2330	unshort 4		norm	0.28	yes	linear drift 0.2 e over 2 days	
	2.8A	C+	NZ 1-19 1-3	6/19 - 6/26/98	inline	Al/AlO$_x$/Al 45 nm/40 mT/75 nm, no grease or paste; 6/17/98		unshort at 4 K?	4 K 6/18 1130			no?	linear but stable over 30 min	3 X 10^{-3}
	2.8B	C+	NZ 1-19 1-3	6/26 - 6/27/98		broke wirebonds before	6/24 350 C N_2	unshort 30 K?				no?	same	1.3 X 10^{-3}
	2.18C	C+	WH67-17 13-16		caged	12/14/99 1400	77 K 1/2 hr 12/15	unshort base	owed 2.18	norm	0.13	**possible**	0.1 e 2 days, mostly flat	1.5 X 10^{-3}
	2.23A	C	WH 72-8 13-15	7/23 - 8/4/00		blanket of AlO$_x$, island on bottom	cold 7/23 1800	unshort base		norm	0.5	**yes**	0.1 e 1 1/2 day	2.0 X 10^{-3}
	2.24A	C	WH 72-13 19-21	8/9 - 8/31/00		8/9/00 1300; blanket center	cold 8/10 2000	unshort base		norm	0.15	strong	0.1 e 1/2 day	1.0 X 10^{-3}
	2.19A	D	WH 72-10 21-24		caged	2/21/00 1800	cold 2/24 1900	unshort 1.6 K		norm	0.5	**yes**	0.1 e 6 hours	2.0 X 10^{-3}
	2.20A	D	WH 72-2 21-24		caged	4 X 10^{-4} ozone TJ, base 1.4 X 10^{-7}	cold 3/14 1800	unshort base		norm	0.38	**yes**	0.1 e 1 day	1.0 X 10^{-3}
	2.24A	F	WH 72-13 22-24			blanket on top of TJs	cold 8/10 2000	unshort base		norm	0.17	? - lots of TLFs		4 X 10^{-3}

TABLE II. Similar to the previous compendium, except that this table is sorted by date of measurement, amongst the devices fabricated at NIST, Gaithersburg. This table is included for two reasons: (1) in order to follow the behavior of a single device when multiple treatments were performed (e.g., Run 2.10) and (2) in order to assess the possiblity that the quality of the drift is correlated with date of fabrication, in case some fabrication parameter (e.g., deposition system base pressure) was drifting over the months or years.

Fab location	Run	Q0 grade	device	meas't dates	notes	fabrication details	pre-condition	pre-cooldown electrical	cooldown details	norm/sc	I_{SD} (nA)	transient?	Q_0 behavior	$\sqrt{S_Q}$ (10 Hz) (e/$\sqrt{\mathrm{Hz}}$)
NIST, G'burg	2.8A	C+	NZ 1-19 1-3	6/19 - 6/26/98	inline	Al/AlO_x/Al 45 nm/40 mT/75 nm, no grease or paste; 6/17/98		unshort at 4 K?	4 K 6/18 1130			no?	linear but stable over 30 min	3×10^{-3}
	2.8B	same	"	6/26 - 6/27/98		broke wirebonds before	6/24 350 C N_2	unshort 30 K?				no?	same	1.3×10^{-3}
	2.10A		SM 1-1 19-21	10/22 - 11/6/98	inline	8/19/1998		unshort 4 K		sc			?	7.5×10^{-4}
	2.10B		"	11/12 - 11/25/98			11/10 350 C H_2		4 K 11/11 2000	"				9×10^{-4}
	2.10C	B-	"	11/27 - 12/9/98			300 K in vac 2 days?	unshort 0.29 K	4 K 11/27 1700	"	0.8	yes (3 days)	best 0.2 e 1/2 day	
	2.10D	B-	"	12/11 - 12/15/98			7 K less than 6 hours	?		"	"	no	0.1 e 1/4 day	
	2.10E	B-	"	12/15 - 12/16/98			40 K less than 8 hrs	?		"	"	no	< 0.1 e 0.2 day	
	2.10F	A-	"	12/17 - 12/30/98			300 K (vac) 8 hrs	left running		"		no	3 TLFs in 14 days (1 in 12 days)	
	2.10G	B+	"	12/31/98 - 1/8/99			300 K (vac) 10? hrs in air 1 hour	short, warm, cool, unshort		"	0.7	no	0.1 e 1 day typical	
	2.10H	B	"	1/13 - 1/14/99			anneal 350 C N_2	short, warm, cool,		"	0.8	no	0.2 e 1 day	
	2.13A	B	SM 3-13 19-21	3/8 - 4/1/99	(angled)	100 nm/65 mT/90 nm hanging by wires; base 9×10^{-6} depo 2×10^{-5}; 3/7/99		unshort 4 K	3/8 1200 77 K 3/9 1100 4 K 4 and 35 K later	sc	0.4	yes	0.1 e 1 day best	
	2.13B	B+	"	4/2 - 4/9/99			300 K (in vac?)	unshort 4 K?		"	"	no	0.1 e 1 1/2 days	
	2.13D	B+	"	4/14 - 4/16/99			300 K (twice)			"	"	no	0.05 e 1 1/2 days	
	2.13E	A-	"	4/30 - 5/6/99			350 C N_2 4/28 1400	unshort 4 K?	two days 100 K	"	"	no	0.1 e 2 days, mostly flat	<~ 4×10^{-4} (not 1/f)
	2.13F	B-	"	5/7 - 5/13/99		rewire 5/7 1100	350 C H_2 5/7 1000	unshort 4 K?	4 K 5/7 1730	"	"	no	0.2 e 2 days, drifting	
	2.14A	A-	SM 3-3 13-15	6/15 - 7/14/99		3/7/98; chip broke once	77 K 3/8/99, dry box 2 1/2 mth, 77 K 5/28 - 6/13	unshorted room temp	77 K 1 day, 4 K, 300 K, base **illuminated**	norm	0.5	no	flat 6 final days	
	2.17	B	WH66-18 5-8	11/12 - 11/19/99	uncaged	10/28/99; base 1.7×10^{-7},	7 days room temp	unshort 4 K.	4 K 3 days?	norm	0.7	no	0.1e 2 days best, lots of drifting	1.0×10^{-3}
		B-	WH66-18 9-12	11/17 - 11/18/99	caged	depo 2.6×10^{-7}	"	"	"	"	0.7		0.2e 1/4 day	
	2.18	A-	WH67-17 17-20	12/22/99 - 1/5/00	uncaged	12/14/99 1400	77 K 1/2 hr 12/15	unshort base	2 K, 300 K, 4 K,	sc	0.13	**NO**	0.1 e 5 days	
		B+	WH67-17 13-16		caged	"	"	"	50 K, base 3 days	"	0.7		drifting, 0.1 e 1 day best	
	2.18C	A-	WH67-17 17-20	2/4 - 2/14/00	uncaged	"	"	unshort base	immediately foll-	norm	0.13	no	0.1 e 4 days	1.0×10^{-3}
		C+	WH67-17 13-16		caged	"	"	"	owed 2.18	"	0.13	**possible**	0.1 e 2 days, mostly flat	1.5×10^{-3}
	2.19A	B+	WH 72-10 17-20	2/23 - 3/13/00	uncaged	2/21/00 1800	cold 2/24 1900	unshort 1.6 K		norm	0.2	no	0.1 e 2 days	1.0×10^{-3}
		D	WH 72-10 21-24		caged	"	"	"		"	0.5	**yes**	0.1 e 6 hours	2.0×10^{-3}
	2.20A	A-	WH 72-2 17-20	3/15 - 4/5/00	uncaged	3/13/00 1100	cold 3/14 1800	unshort base		norm	0.14	no	0.1 e 5 days	0.5×10^{-3}
		D	WH 72-2 21-24		caged	4×10^{-4} ozone TJ, base 1.4×10^{-7}	"	"		"	0.38	**yes**	0.1 e 1 day	1.0×10^{-3}
	2.22A	B	WH 79-16 13-15	7/12 - 7/18/00	inline	7/11/00; base 6×10^{-6}	cold 7/22 2200	unshort base		norm	0.03	no	0.1 e 1 day	
		B-	16-18			"	"	"		"	0.03	no	0.1 e 0.5 day	
	2.23A	C	WH 72-8 13-15	7/23 - 8/4/00		blanket of AlO_x, island on bottom	cold 7/23 1800	unshort base		norm	0.5	**yes**	0.1 e 1 1/2 day	2.0×10^{-3}
		B	16-18			7/22/00; no blanket	"	"		"	0.18	no	0.1 e 3 days	0.7×10^{-3}
	2.24A	C	WH 72-13 19-21	8/9 - 8/31/00		8/9/00 1300; blanket center	cold 8/10 2000	unshort base		norm	0.15	strong	0.1 e 1/2 day	1.0×10^{-3}
		F	22-24			blanket on top of TJs	"	"		"	0.17	? - lots of TLFs		4×10^{-3}
	2.25A		WH 72-21 10-12	9/29 - 10/17/00		9/29/00 1100; no blanket	cold 9/29 2330	unshort 4 K		norm	0.26	no		
			7-9		"	blanket center, island on top	cold 9/29 2330	"		"	0.28	yes		
PTB	2.42B, C	A-	SL-66 44	8/11 - 8/27/05	inline	Al 150 nm, 1997		unshort 4 K	4 K, 300 K air, 4 K	norm	0.14	no	0.15 e 9 days	
NIST, Boulder	2.45	B	6-3-05 1	11/4 - 11/12/05		6/3/2005		unshort 4 K	none	norm	5.1	no	linear drift 0.1 e over 2 days	

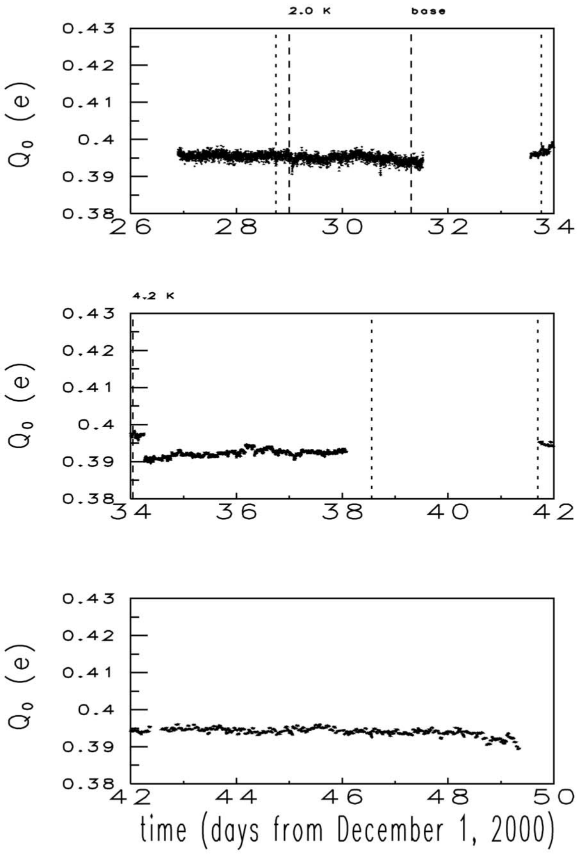

FIG. 6. An example of $Q_0(t)$ for a Si device, using method II; note the scale change (previous figures had a range from 0 to 1e, while here the range is 0.05e) (Si/SiO_2). As in previous plots, dotted lines denote transfers of liquid He, and dashed lines refer to specific temperature excursions. Over the entire 22 day period, the difference between minimum and maximum values of Q_0 is 0.010e. We note that much of this change was caused by the rise in temperature to 4.2 K. Data correspond to run 2.26A in Table III.

quite stable over time. An example is shown in Fig. 6. This behavior is clearly different from, and qualitatively better than, $Q_0(t)$ in the metal-based devices.

We note that this measurement was taken using the same measurement system (in NIST, Gaithersburg, MD, USA) as were all of the measurements on the metal-based transistors. Thus, the poor results for $Q_0(t)$ presented in the previous section on the metal-based devices are unlikely to be due to some external source of noise or perturbation in the particular measurement system used.

Table III, similar to the previous tables, shows a compendium of the results that we have obtained for $Q_0(t)$ on the Si devices that we have measured. In general, the devices showed a lack of significant charge offset drift. We note that, since the various devices listed were fabricated in two different locations, it is unlikely that the excellence of the $Q_0(t)$ behavior is due to the particular conditions at one of the fabrication locations.[14] In addition, we note that even after "training" the device (applying voltage pulses to the drain and gate),[10] the charge offset drift was quite small. We also note that the level of short-term noise at 10 Hz, when measured free of the rare TLFs, is similar to that in the metal-based devices.[10]

B. Stability of TLFs in Si-based devices

A common observation in the field, of which an example is shown in Fig. 4, is that TLFs in metal-based devices are typically unstable: They appear and disappear in an uncontrolled fashion as a function of either time, thermal cycling, or electrostatic discharges. In contrast, in the Si-based devices, the TLFs appear to be completely stable as a function of all of these parameters.

For examples of the stability of TLFs, we can show data from a particular Si-based device which showed Coulomb blockade up to room temperature. Before showing the stability, we start by demonstrating the basic operation over the temperature range: Figure 7 shows the drain current versus gate voltage at various temperatures for this device. This device likely had an unintentional tunnel junction which caused the nonperiodic dependence; it also apparently substantially reduced the total size of the device, thus making it possible to see at least one Coulomb blockade peak (at a gate voltage between 3.4 and 3.5 V) up to room temperature.

TABLE III. Compendium of measurements on Si-based devices, fabricated at NTT, Tokyo, Japan and at Cornell University/NIST Gaithersburg, both of USA. In contrast to the metal-based devices (Table II), the Si-based devices show no significant charge offset drift. Notes: PADOX, V-PADOX, and "tunable" refer to various device architectures (Ref. 2 and 27).

Fab location	Run	device	meas't dates	notes	pre-cooldown electrical	cooldown details	meas't T (K)	I_{SD} (nA)	$\lvert Q_0^{max} - Q_0^{min} \rvert$; number of days	$\sqrt{S_Q}$ (10 Hz) ($e/\sqrt{Hz}$)
NTT, Japan	2.26A	2D-3Y	12/27/00 - 1/19/01	PADOX	unshort 4 K	3 hours from 77 to 4 K	base to 4.2 K	50	0.010 e over 22 days	5 X 10^{-5}
	2.27A1	2B-1Y	2/2/01 - 2/23/01	"	"	43 hours from 300 to 4 K	4.2 K	30	0.008 over 21 days	
	2.27A2	"	2/23/01 - 3/1/01	"	voltage pulses V_{SD} ± 20 mV, V_G ± 10 V	stayed at 4 K	"	"	0.03 e over 6 days	
	2.30A	2B-2Y	4/16/02 - 4/22/02	V-PADOX	unshort 4 K				0.004 e over 4 days	3 - 4 X 10^{-5}
	2.46	AF-CA2R3D-1	5/2/06 - 5/5/06	tunable	unshort 4 K		base	0.04	0.013 e over 2.5 days	
	2.47	"	4/27/06 - 5/10/06	"	"		"	0.02	0.08 e over 4.5 days	
	2.48	AF-CA2R3C-2	6/9/06 - 6/24/06	"	"		"	0.01	0.015 e over 11 days	
	2.51	AF-CA2C3C	8/706 - 8/23/06	"	"		0.2 to 1.4 K	0.05	0.015 e over 16 days	
NIST, USA	2.54	JW1.7-24-SDEL	12/9/06 - 1/13/07	"	"		base, 4 K to 17 K	25	0.01 e over 4 days, 0.04 e over 35 days	
	2.55	JW2.4-23-EL	5/18/07 - 5/30/07	"	unshorted during cooldown		base to 1.1 K	0.5	0.03 e over 13 days	

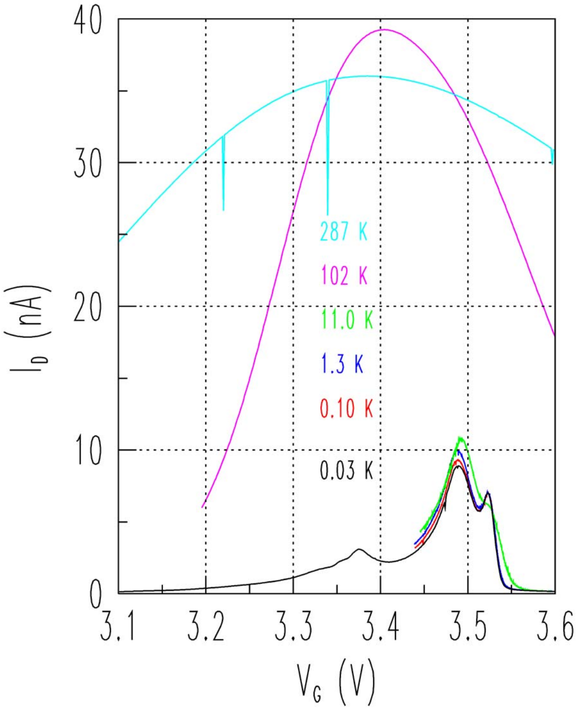

FIG. 7. (Color online) Dependence of drain current on gate voltage for device 2C-1Y (Si/SiO_2). This device likely had an unintentional tunnel junction which reduced the total size of the device, thus making it possible to see at least one Coulomb blockade peak up to room temperature. At the highest temperature, the downward spikes are due to a single dominant TLF.

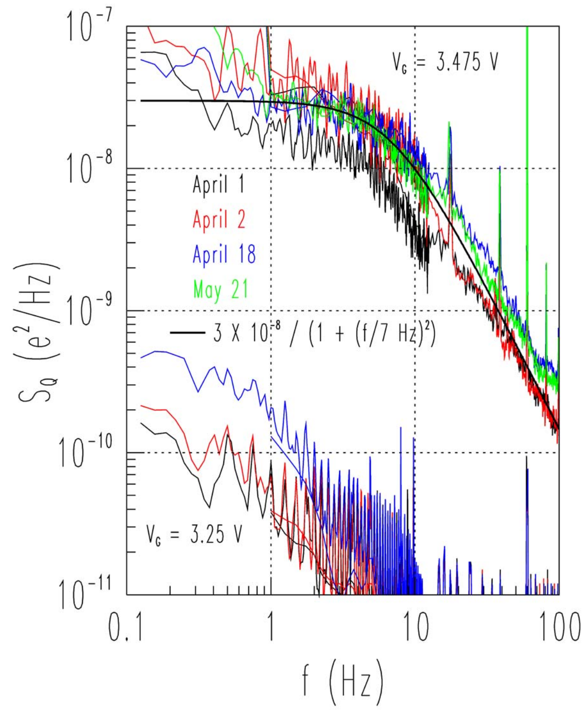

FIG. 8. (Color online) Power spectral density of charge fluctuations vs frequency at the base temperature (0.02–0.04 K), for the same device as in Fig. 7; various colors refer to four different measurement dates (Si/SiO_2). At these temperatures, there was a single dominant TLF at V_G=3.475 V, which was absent at V_G=3.25 V. The stability of this TLF is demonstrated by both the extended period of time during which it was present, as well as the fact that there were multiple thermal cycles up to room temperature between the various measurements.

As the first example of the stability of the TLFs in Si-based devices, we show the power spectral density of charge fluctuations in this device near the base temperature (see Fig. 8). In this temperature range, there was a single dominant TLF which was highly gate-voltage-dependent. Thus, the curves at V_G=3.475 V show the characteristic Lorentzian shape [$S \propto 1/(1+(f/f_0)^2)$, see the fit in Fig. 8] for a two-level fluctuator;[17] in contrast, the curves at V_G=3.25 V show typical $1/f$ noise at a much lower amplitude. Note that, over the course of 1 1/2 months, the TLF has changed in neither amplitude or knee frequency f_0. We note that there were two thermal cycles up to room temperature between the measurements shown.

As a second example of the stability (in Fig. 9), we show $I_D(V_G)$ for temperatures near 70 K. In this temperature range, there was another stable TLF which moved through the bandwidth as a function of temperature. Again, between the two sets of curves shown, there were both multiple thermal cycles up to room temperature as well as an extended period of time (four months).

C. Full range of $S_Q(f,T)$

We also take the opportunity, which is possible only because of the presence of Coulomb blockade up to room temperature, to present the temperature dependence of the power spectral density of charge fluctuations over the entire temperature range (see Fig. 10). We note that each peak in the noise at 1 Hz, as a function of temperature, corresponds to a TLF, with a Lorentzian lineshape in the noise spectrum; the amplitude in the troughs is the background $1/f$ noise level.

Finally, we note that although the large charge offset drift in metal-based devices is the appropriate figure of merit for integration, we can also compare noise levels in both types of devices in the context of the noise floor for use as an electrometer. In that context, we note that both metal- and Si-based devices have $\delta Q_0 \leqslant 10^{-3}e$ in the audio range (based on the short-term $1/f$ noise); in contrast, $Q_0(t)$ shows that Si-based devices have about the same fluctuation size at much lower frequencies (about 10 μHz), while metal-based devices have $\delta Q_0 \approx 1e$ at that frequency.

IV. MODEL FOR CHARGE OFFSET DRIFT

In the previous two sections, we have shown convincing evidence that the charge offset drift in Si-based devices is orders of magnitude smaller than in metal devices, while the level of $1/f$ noise is about the same. In addition, we have also shown another empirical difference: The TLFs in the Si-based devices are very stable over time and thermal cycling, while those in the metal-based devices are notoriously unstable.

Thus there arises a natural question: What is the difference between these two classes of devices? More specifically, can we understand the origin of the charge offset drift in the metal-based devices? In this section, we use the results of the established field of TLSs (Ref. 15) in glassy and amorphous materials to develop a prediction for the charge offset drift.

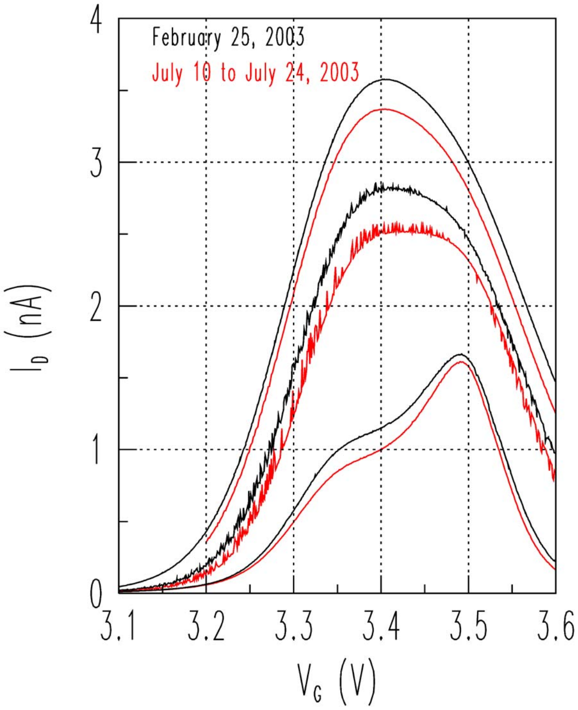

FIG. 9. (Color online) A single Coulomb blockade peak for temperatures between 37 and 89 K, for the same device as in Fig. 7 (Si/SiO_2). In this range, there was a single dominant TLF (indicated by the large additional amount of noise on the middle pair of curves) which moved through the bandwidth as a function of temperature. Upper pair: 89 and 80 K. Middle pair: 69 and 62 K. Lower pair: 41 and 37 K. As in Fig. 8, the stability of this TLF is demonstrated by both the long period of time between the first set of measurements and the second, as well as by the multiple thermal cycles up to room temperature between the two sets of measurements.

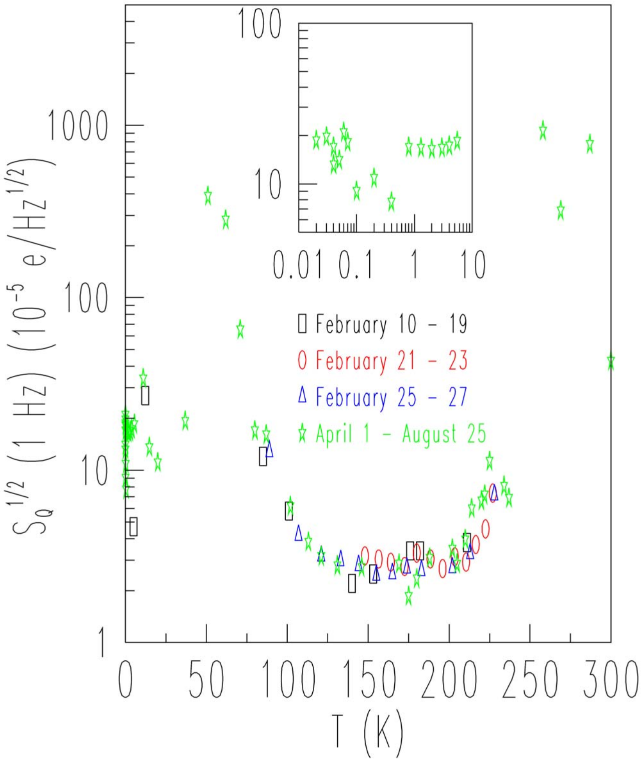

FIG. 10. (Color online) Temperature dependence of the amplitude of power spectral density fluctuations measured at 1 Hz and V_G in the range of 3.4–3.5 V, over various periods of time, for the same device as in Fig. 7 (Si/SiO_2). Main: The peaks at about 60 and 270 K correspond to dominant TLFs, with a Lorentzian power spectral density; the rest of the data corresponds to typical $1/f$ noise. Note that these two TLFs were stable over long periods of time as indicated by the repeated measurements of the same peaks. Inset: At low temperatures, there were two TLFs dominant, below 0.1 and between about 1 and 10 K. In contrast to the two TLFs at higher temperatures, these two were much less temperature dependent, although they were highly gate-voltage-dependent.

We base our model on one of the standard observations in the TLS field: the nonequilibrium heat evolution from glasses. For example, in silica glass[18] held at an "annealing" temperature near 1 K, and then quenched to 0.2 K, a calorimetry measurement showed a long-time tail (after the exponential falloff due to the RC time constant) to the heat evolving from the glass; this tail was proportional to 1/time. We argue that the same type of nonequilibrium relaxation of charged defects in the insulating regions surrounding the SET island of the metal-based devices leads to the charge offset drift that we see.

The standard theory,[19,20] which accounts naturally for the nonequilibrium heat evolution, contains the idea that by allowing heavy-atom tunneling we can understand how the structural matrix of glass can be in motion even at very low temperatures (near 1 K). This model considers a distribution of double-well potentials, with asymmetry Δ and tunneling energy Δ_0. Following the theory of Black,[21] we use a distribution of TLS,

$$n(E,t) = (\bar{P}/2)\ln(4t/T_{1,\min}(E)),$$

where $\bar{P}$ is the "universal" TLS density of states,[22] t is the running time, $T_{1,\min}^{-1}$ is the minimum TLS-phonon relaxation rate, and $E=\sqrt{\Delta^2+\Delta_0^2}$. Then, the rate of arrival of energy packets with energies between $E_{\min}$ and $E_{\max}$ (V is sample volume) is as follows:

$$\dot{N} = V d/dt \int_{E_{\min}}^{E_{\max}} dE\, n(E,t) = V \int_{E_{\min}}^{E_{\max}} dE\, dn(E,t)/dt$$

$$= V \int_{E_{\min}}^{E_{\max}} \bar{P}/(2t),$$

$$\dot{N} = V\bar{P}(E_{\max} - E_{\min})/(2t). \tag{1}$$

In order to make contact with the charge offset drift $Q_0(t)$, we must make some assumptions:

(1) The most significant assumption is simply that every relaxation event of a TLS is electrostatically coupled to Q_0; to put this a different way, we are assuming that every TLS has a dipole moment which changes when it relaxes. This assumption will result in an overestimate for the rate of charge offset drift.
(2) $E_{\min}=0$, and $E_{\max}=0.1$ eV. The latter value we obtain by assuming that any structural reconfiguration can contribute to the charge offset value, and thus that all energies up to the approximate lattice binding energy are available.
(3) We obtain the volume V by assuming that there is a "skin" of amorphous AlO_x on the surface of the SETT

islands (area of 0.1 μm^2) with a thickness of 2 nm, and that the AlO_x has the same density of TLS ($\bar{P} \approx 5000\ K^{-1}\ \mu m^{-3}$) and energy release as the vitreous silica.[18]

(4) We assume $t=2$ months.

We wish to comment on this last assumption of the running time t. In the nonequilibrium heat evolution experiments, the evolution recurs each time the sample is warmed to a few kelvins and then quenched. In contrast, as we noted previously, the nonequilibrium transient relaxation that we see in $Q_0(t)$ does not recur upon thermal cycling; instead, it appears to be associated with time since fabrication. We thus speculate that the nonequilibrium TLS relaxation is associated with a nonequilibrium structural condition (examples might include OH^- in the AlO_x or built-in film stresses) that occurred at the time of device fabrication. This interpretation of our experimental results motivates both our estimate for E_{max} and our estimate for t; in this interpretation, the reason for the nonrecurrence of the transient relaxation is that the nonequilibrium structural condition will not be reproduced by thermal cycling. We expect to analyze in more detail both the prediction and our experimental results for the transient relaxation of $Q_0(t)$ in a subsequent publication.

With regards to the *value* of 2 months: This value is a median for the time between fabrication and measurement, as can be seen by examining the tables. We specifically note that the time between fabrication and measurement for the PTB device (eight years) is much longer than this; this is consistent with the fact that the drift behavior for the PTB device was as good as any other metal-based device, as seen in the tables.

With the above assumptions, we can proceed to obtaining a numerical estimate for the time rate of charge offset changes that will lead to the hysteretic jumps and smooth drift evident in $Q_0(t)$:

$$\dot{N} = (0.1\ \mu m^2)(0.002\ \mu m)(5100\ K^{-1}\ \mu m^{-3})(1000\ K)/(2) \times (1440\ h),$$

or

$$\dot{N} \approx 1/(3\ \text{hours}).$$

We note that this estimate is probably an upper bound, due to the assumption that every TLS relaxation corresponds to a charge polarization change on the SETT island. Given these caveats, the numerical agreement seems quite compelling between this estimate and our experimental observations that there is typically a hysteretic jump in Q_0 once every few days.

Now that we have developed our model and the numerical estimate for a disordered material, we can also return to the question posed at the beginning of this section: Why is the drift in the Si-based devices so much smaller than in the AlO_x-based ones? In the context of our model, the answer is now clear: In the standard model for the behavior of glassy materials,[15] the general behavior and specifically the nonequilibrium heat evolution come from the complicated dynamics of a large number of interacting defects; these interactions result in a large phase space in which the motion of any one defect depends on the configuration of a number of other defects. For our measurements, an example of this is the instability of the TLFs in the metal devices, which we can now interpret as being due to change in the configuration of other defects whose dynamics are not visible through the charge noise. In contrast, for the Si devices, the stability of the TLFs clearly indicates that there are in general no interactions between separate TLFs, unlike in the metal devices; thus, since the interactions are what give rise to the glassy relaxation, the stability of the TLFs explain why there is no corresponding long-time charge offset drift.

V. DISCUSSION AND CONCLUSIONS

We can summarize what we believe are the most important results of this work:

(1) To date, the search for a metal-based SET device that lacks charge offset drift has not been successful.
(2) In order to demonstrate a lack of charge offset drift, comprehensive measurements over an extended period of time are necessary.
(3) Although noise-producing defects (TLFs) exist in Si-based SET devices, there is no measurable charge offset drift in these devices.
(4) The crucial difference between these two classes of devices appears to be the *stability* of the TLFs in the Si-based devices.
(5) A model based on the observation of nonequilibrium relaxation in amorphous materials yields a numerical estimate for the rate of charge offset drift which is quite close to the observations.

From these results, we can conclude that the crucial difference between Si-based and metal-based SET devices is in the stability of the TLFs rather than that the Si-based devices are perfect with absolutely no defects. This conclusion leads to a natural suggestion for future work in this field: In order to obtain metal-based devices without charge offset drift, we should concentrate more on fabrication processes that avoid interaction between defects rather than focusing solely on trying to reduce the density of defects.

Based on the combination of our model for the drift, the time dependence of the transient relaxation, and the differences between Si and AlO_x devices, we can speculate on possible materials-specific causes for the drift.

a. OH^-. One important difference between the Si-based and the AlO_x-based devices is that the tunnel barriers are buried in and surrounded by crystalline Si in one case, whereas they are on the surface of the device in the other case. This suggests that impurities, and specifically the hydroxyl ion which is known to be incorporated into the AlO_x during deposition, may play a role. As we emphasized in the discussion of our model, the nonequilibrium nature of this impurity, and in particular that its density may change over time since fabrication as it diffuses out, would lead to the observation of drift. More generally, the presence of any surface adsorbate would lead to a similar conclusion.

b. Density of Al in AlO_x. The process of oxidation of Al, as described in the Cabrera–Mott model,[23] involves diffusion of the Al ions from the bulk metal up through the graded oxide to the surface, where those ions combine with O^- ions to form the oxide; this process will naturally give rise to a gradient of stoichiometry. As in the previous discussion, this gradient is not in thermodynamic equilibrium, and thus can give rise to time-dependent relaxation since the fabrication time.

c. Condensed metal droplets. There is some anecdotal evidence that due to the specific fabrication process of the AlO_x-based devices,[24] there can be a gradient of Al deposition beyond the defined edge of the lithographic pattern. This gradient will naturally give rise to a metal island film, with isolated small metal particles in an insulating matrix. These isolated particles could then clearly leak charge back and forth slowly over time. We note that this leakage could occur as a result of a change in a nearby electrode voltage, in addition to as a function of time since fabrication; such an observation (change in the drift behavior with applied voltage) has not typically been seen by us.

d. Film mechanical stress. Due to the deposition of evaporated metal onto a room-temperature substrate, deposited films often have a large amount of built-in nonequilibrium stress which could relax over time since fabrication.

Given the speculations, we can suggest various fabrication improvements which might reduce or eliminate the drift problem: (1) To alleviate the problems of density gradient, condensed metal droplets, and possibly the hydroxyl ion and film stress issues, we note that much progress has been made recently on developing a fabrication process which produces crystalline Al_2O_3 (on a lattice-matched substrate) rather than amorphous AlO_x.[25] (2) To alleviate the problem of impurities, it might be fruitful to try depositions in better vacuum chambers with lower vacuum pressure. (3) To avoid built-in stress, one can deposit the Al onto a heated or lattice-matched substrate.

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